

AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph at page 8, lines 9-20, as follows:

FIG. 4 illustrates a global routing multiplexer 20 that has the capability to realize any permutation of a given length of inputs, namely to interconnect the inputs with outputs in some specified, permuted order. Multiplexer 20 has control inputs 22 for control bits as well as n inputs 24 and n outputs 26 to be interconnected in an order specified by the control bits at inputs 22. As shown in FIG. 4, inputs $0, 1, \dots, n-1$ are transformed to outputs $0, 1, \dots, n-1$ in a permuted order, ~~which in the example of FIG. 4 shows input 0 connected to output 1, input $n-1$ connected to output 2, etc.~~